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From: **Sumit Bhattacharya** **Date:** **March 17, 2005**
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Docket Number: **2207/10083** **Total number of pages:** **5**
(including cover)

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Ex. Guy J. LAMARRE Group Art Unit 2133	U.S. Patent and Trademark Office	703-872-9306	

Message:

Application No. : 09/751,750 Confirmation No. 5033

Applicant : Talal K. JABER

Filed : December 29, 2000

Title : MICROPROCESSOR ON-CHIP TESTING ARCHITECTURE AND IMPLEMENTATION

TC/A II : 2133

Examiner : Guy J. LAMARRE

PAPER(s) ENTITLED: **Notice of Appeal (in duplicate)** **2 pages**
 Request for Extension of Time (in duplicate) **2 pages**

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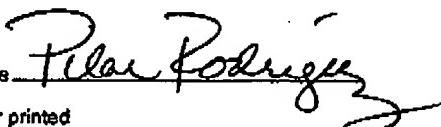
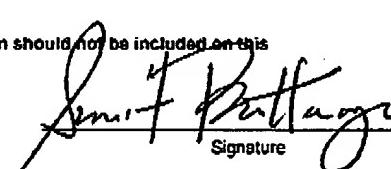
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PTO/SB/31 (08-03)

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For Microprocessor On-Chip Testing Architecture And Implementation									
Art Unit 2133	Examiner Guy J. LAMARRE								
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In re Application of

Talal K. JABER

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Art Unit
2133Examiner
Guy J. LAMARRE

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I am the

- applicant/inventor.
- assignee of record of the entire interest. See 37 CFR 3.71.
- Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- attorney or agent of record.

Registration number 51,469

- attorney or agent acting under 37 CFR 1.34(a).

Registration number if acting under 37 CFR 1.34(a). _____

Signature

Sumit Bhattacharya

Typed or printed name

(408) 975-7500

Telephone number

March 17, 2005

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

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